

REMARKS

Claims 1-22 are pending in the application.

Claims 1-22 are rejected.

Claims 1-9, 11-18, and 22 have been amended.

No new matter is added.

Reconsideration and allowance of claims 1-22 is respectfully requested for the reasons set out below.

Informalities

In the claims, the word "assistant" has been replaced with "pilot" to better represent the meaning of the claims. *The American Heritage® Dictionary of the English Language, Third Edition* (copyright © 1992 by Houghton Mifflin Company) defines *pilot* as "the relatively small heading or excavation first made in the driving of a larger tunnel." Clearly, this is the intended meaning of the term *assistant* in the context of the instant disclosure and claims. Specifically, the assistant trench (107, FIG. 3) is formed initially to assist in the formation of the intended final trenches, namely the upper and lower trenches (122 and 123, respectively). Because of this role of the assistant trench (107), in view of the dictionary definition recited above, a better term to accurately convey meaning is *pilot trench* (107).

It is noted that a clerical error in the specifications has been corrected. At page 7, line 15, the number 115 was changed to 116.

Claims 11 and 14 are rejected based upon informalities and indefiniteness. These claims have been amended to eliminate the informalities and indefiniteness noted by the examiner.

Claims 1-5 and 8-11 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 6,144,086 to Brown, et al. ("Brown"). The rejections are respectfully traversed.

Brown shows a semiconductor device with a dual depth trench. The trench shown in Brown has a wide upper portion and a narrow lower portion.

The applicant's device includes a semiconductor substrate with a cell region and a high voltage region. As shown in Figures 3-5, the cell region is designated "c" and the high voltage region is designated "d". The applicant's device has a cell trench 120 in the cell region

and a dual width trench 125 in the high voltage region. The same etching step is used to form the trench in the cell region and to form part of a dual depth trench in the high voltage region. That is, the trench in the cell region and a part of the dual depth trench in the high voltage region are concurrently etched.

Claim 1 (and therefore dependent claims 2-11), as amended, in part recites the semiconductor substrate including "a cell region and a high voltage region". Claim 1 further recites:

"concurrently forming an upper trench, a bottom trench, and a trench in the cell region, the upper trench substantially centered at the location of the pilot trench, the bottom trench having a top at substantially the same level as a bottom surface of the upper trench, and the upper trench having a wider width than that of the bottom trench"

Thus, three trenches are formed in one step. Since the same step forms the three trenches, the size of the trenches can be coordinated and controlled.

In contrast, Brown merely shows one trench that has a wide upper portion and a narrow bottom portion. Brown does not teach or suggest simultaneously making trenches in both a cell region and in a high voltage region as claimed by the applicant. Reconsideration of this rejection and allowance of these claims is therefore respectfully requested.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown, et al. in view of Ohno (US Patent 6,586,295). The rejections are respectfully traversed.

Ohno shows a doping method. Ohno does not suggest simultaneously forming trenches in a cell region and in a high voltage region of a substrate. Allowance of claim 6 and 7 is requested based on the same reasoning as explained above in regards to claims 1-5 and 8-11.

Claims 12-16 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown, et al. in view of Bohr (US patent 5,536,675).

The above discussion of the Brown reference is also applicable to this rejection of claims 12-16 and 19-21. The Bohr reference describes a process of first forming two trenches and then employing a separate step to form a deep trench.

Applicant's claim 12 (and thus dependent claims 13-21) as amended recites:

"forming in a single step, a first trench in said first region and enlarging said pilot trench to form a second trench composed of an upper trench and a bottom trench at the bottom of the upper trench"

With the applicant's invention, a single step is used to form the trench in the first region and to enlarge the trench in the second region to form an upper trench and a bottom trench. This provides a simpler process and allows better control than is possible with the prior art. The combination of Brown and Bohr do not contain all of the elements recited in claim 12. Reconsideration and allowance of independent claim 12 and dependent claims 13-21 is therefore requested.

Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown, et al. and Bohr as applied to claim 14 above, and further in view of Ohno.

The above discussion of Brown, Bohr and Ohno is equally applicable to rejection. Allowance of these claims is requested for the same reasons as discussed above.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brown, et al. in view of Bohr and Lee, et al.

The Brown and Bohr references were discussed above and that discussion of those references is also applicable to this rejection.

The Lee reference, as noted by the examiner, shows forming a key trench in a key region.

Claim 22 recites forming a trench in a key region. However, claim 22 also recites

"anisotropically etching the bottom surface of the pilot trench and the exposed semiconductor substrate to form a first trench at the first region, a second trench composed of an upper trench at a surface of the semiconductor substrate at the second region and a bottom trench at a bottom surface of the upper trench, and a key trench composed of an upper key trench at a surface of the semiconductor substrate at the key region and a bottom key trench at a bottom surface of the upper key trench".

In the etching step quoted above, in addition to forming a key trench, the above quoted step forms:

"a first trench at the first region, a second trench composed of an upper trench at a surface of the semiconductor substrate at the second region and a bottom trench at a bottom surface of the upper trench".

No such step is shown or suggested in the cited references. Allowance of claim 22 is therefore respectfully requested.

For the foregoing reasons, reconsideration and allowance of claims 1-22 as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



Hosoon Lee
Reg. No. 56,737

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613
Customer No. 20575

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Li Mei Vermilya